

<b>INFORMATION DISCLOSURE CITATION</b> FEB 24 2005 PATENT & TRADEMARK OFFICE TO-1449		<b>Complete If Known</b>	
		Application Number	10/662,204
		Filing Date	September 12, 2003
		First Named Inventor	Nguyen et al.
		Art Unit	2819
Examiner Name	Cho, James Hyonchol	Attorney Docket Number	60809-0127-US
Sheet		of	2

U.S. PATENT DOCUMENTS						
Examiner Initials	Document Number Number - Kind Code <sup>1</sup>	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Class	Subclass	Filing Date if Appropriate
Jc	5,182,467	01/1993	Taylor et al.	327	175	
Jc	5,194,765	03/1993	Dunlop et al.	326	87	
	5,254,883	10/1993	Horowitz et al.	326	30	
	5,373,477	12/1994	Sugibayashi, Tadahiko	327	541	
	5,430,400	07/1995	Herlein	327	108	
	5,530,377	06/1996	Walls	326	30	
	5,783,956	07/1998	Ooishi, Tsukasa	327	143	
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	5,847,578	12/1998	Noakes et al	326	39	
	5,933,051	08/1999	Tsuchida et al.	323	315	
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Jc	6,661,268	12/2003	Stark et al.	327	170	

FOREIGN PATENT DOCUMENTS							
Examiner Initials	Foreign Patent Document Country Code <sup>2</sup> - Number <sup>3</sup> - Kind Code <sup>4</sup> (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Class	Subclass	Translation	
						Yes	No
Jc	EP 0 463 316 A1	01/02/1992		H04L	12/40	✓	
Jc	EP 0 482 392 A2	04/29/1992		H04L	25/08	✓	
Jc	JP 58-54412 (A)	03/31/1983		G05F1	56		abstract only

OTHER PRIOR ART - NON PATENT LITERATURE DOCUMENTS	
Examiner Initials	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published
	Allen, Arnold O., "Probability, Statistics, and Queuing Theory with Computer Science Applications", 2nd Edition, CH 7, pp 450, 458-459
Jc	Chappell, Terri I. et al., "A 2ns Cycle, 4ns Access 512 kb CMOS ECL SRAM", <i>IEEE International Solid State Circuits Conference</i> , 1991, pp 50-51
Jc	Donnelly, Kevin S. et al., "A 660 MB/s Interface Megacell Portable Circuit in 0.3 μm-0.7 μm CMOS ASIC", <i>IEEE Journal of Solid State Circuits</i> , 31(12):1995-2003 (1996)

Examiner Signature	James Cho	Date Considered	8/21/05
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<b>INFORMATION DISCLOSURE CITATION</b>  PTO-1449				<b>Complete If Known</b>	
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				<b>Examiner Name</b>	Cho, James Hyonchol
<b>Sheet</b>	2	of	2	<b>Attorney Docket Number</b>	60809-0127-US
<i>h</i>	Pilo, Harold et al., "A 300 MHz 3.3V 1 Mb SRAM Fabricated in a 0.5 $\mu$ m CMOS Process", <i>IEEE International Solid State Circuits Conference</i> , pp. 148-149 (1996)				
<i>h</i>	Schumacher, Hans-Jürgen et al., "CMOS Subnanosecond True-ECL Output Buffer", <i>IEEE Journal of Solid-State Circuits</i> , <b>25</b> (1):150-154 (1990)				
	Sidiropoulos, Stefanos et al., "A 700-Mb/s/pin CMOS Signaling Interface Using Current Integrating Receivers", <i>IEEE Journal of Solid-State Circuits</i> , <b>32</b> (5):681-690 (1997)				
	Yang, Tsen-Shau et al., "A 4-ns 4Kx1-bit Two-Port BiCMOS SRAM", <i>IEEE Journal of D-State Circuits</i> , <b>23</b> (5):1030-1040 (1988)				
<i>h</i>	EIA/JDEC, JC-42.3 Committee on RAM Memories, Minutes of Meeting 63, July 21, 1992, Denver, CO.				
<i>h</i>	EIA/JDEC, JC-42.3 Committee on RAM Memories, Minutes of Meeting 64, Sept. 16-17, 1992, Crystal City, VA.				

<b>Examiner Signature</b>	<i>James Cho</i>	<b>Date Considered</b>	<i>8/2/05</i>
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